ABSTRACT

An insulation layer is formed on the substrate of a semiconductor wafer. A bottom electrode is formed on the surface of the insulation layer followed by forming a dielectric layer to cover the bottom electrode. Thereafter, an etching process forms an upper electrode hole within the dielectric layer to connect to the surface of the bottom electrode. A spacer is formed around the walls within the upper electrode hole. A capacitor dielectric layer is then formed on the surface of the dielectric layer, on the bottom within the upper electrode hole, and on the spacer. Finally, an upper electrode is formed within the upper electrode hole to complete fabrication of a capacitor.